

**University of Bahrain**  
**College of Information technology**  
**Department of Computer Engineering**

**Test (2)**

Student Name	
I.D. No.	
Section	

**Course Title:** Digital Logic  
**Course number:** ITCE 202/250  
**Semester:** 1  
**Academic Year:** 2012/2013  
**Duration :** 1 hour  
**Date:** 14<sup>th</sup> May 2013

*Solution*

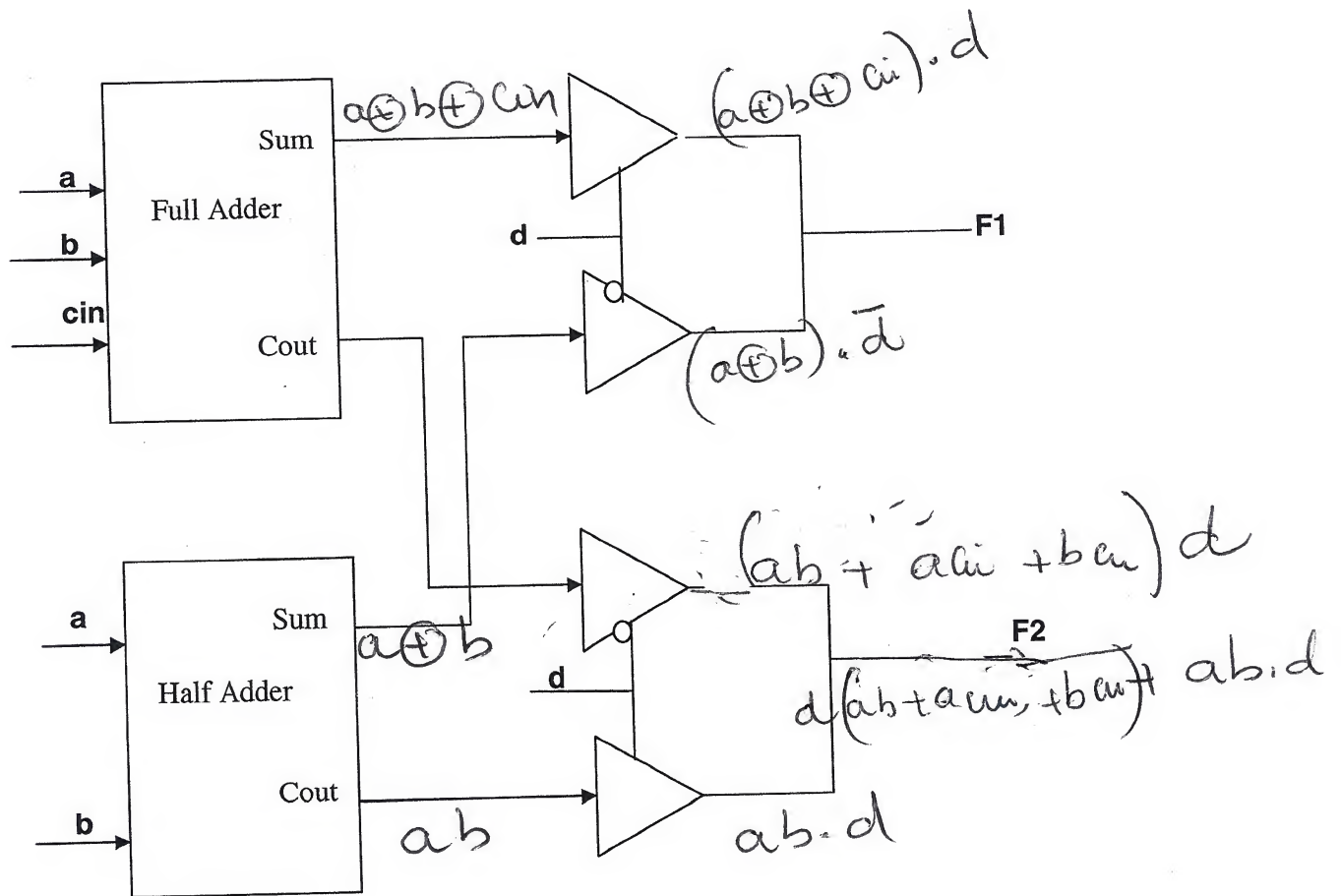
**Read the following before you start:**

1. Write your name, ID and section number
2. Answer all questions.
3. Write your answers on the attached sheets only.

Question	Mark	Mark attained
1	12	
2	12	
3	12	
4	12	
5	12	
Total	60	

**Question [1]: [ 12 mark]**

Write the equations of the functions F1 and F2 generated by the following circuit.

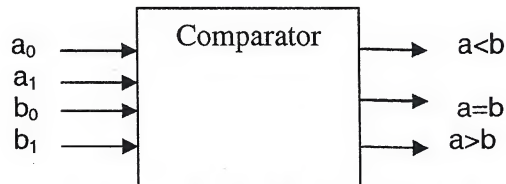


$$F_1 = (a \oplus b \oplus cin) \cdot d + (a \oplus b) \cdot \bar{d}$$

$$F_2 = (ab + acin + bcin) d + ab \cdot d$$

**Question [2] : [12 marks]**

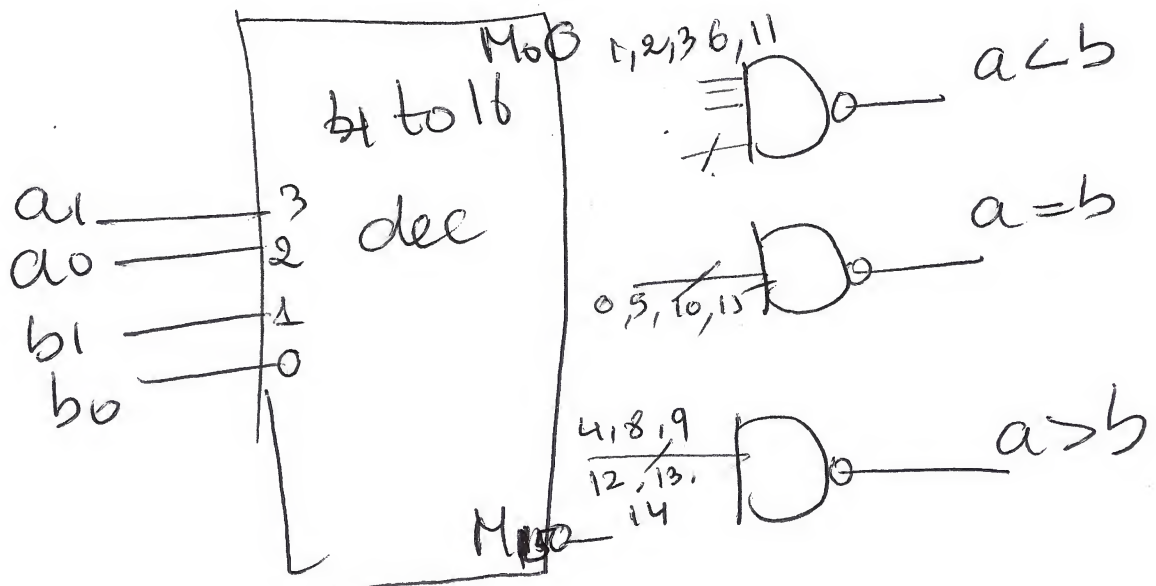
We want to design a 2-bit word comparator that compares the word  $a = a_0 a_1$  with the word  $b = b_0 b_1$ .



1) Give the truth table of the comparator.

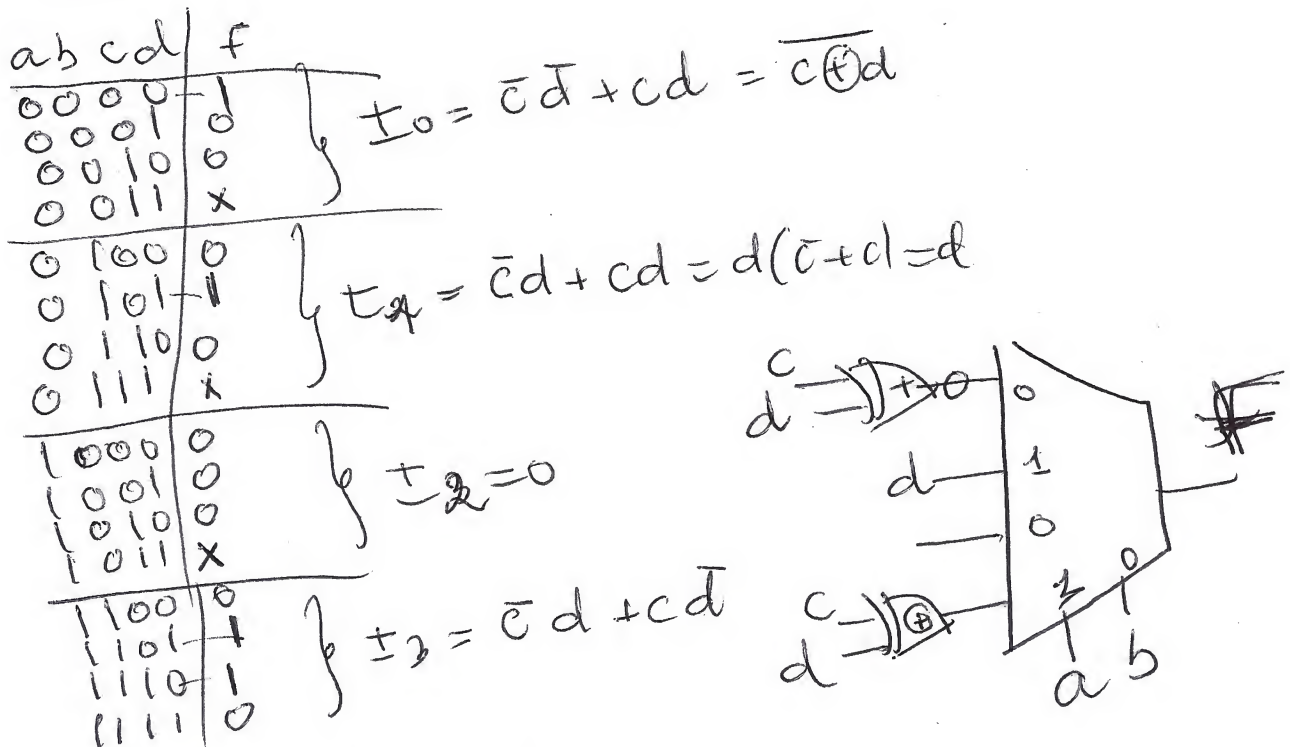
$a_1 a_0$	$b_1 b_0$	$a < b$	$a = b$	$a > b$
00	00	0	1	0
00	01	0	0	0
00	10	0	0	0
00	11	0	0	0
01	00	0	0	0
01	01	0	1	0
01	10	0	0	0
01	11	0	0	0
10	00	1	0	0
10	01	1	0	0
10	10	1	0	0
10	11	1	0	0
11	00	1	0	0
11	01	1	0	0
11	10	1	0	0
11	11	0	1	0

2) Implement the comparator with a decoder with inverted outputs and only NAND gates.

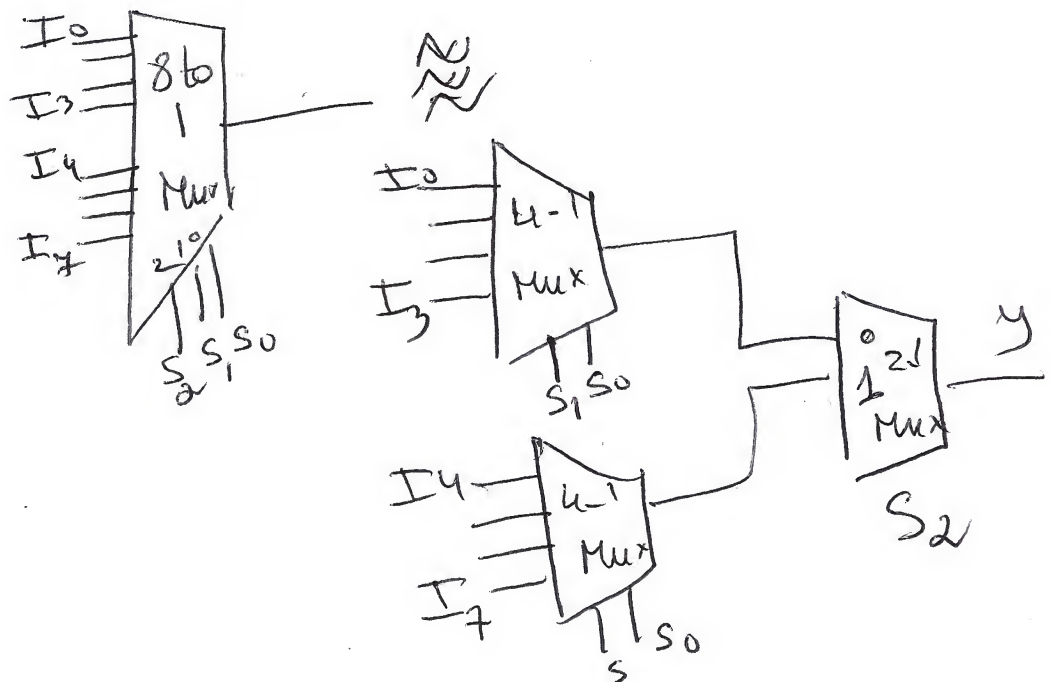


**Question [3]: [ 12 marks]**

- a. Implement  $F = \Sigma m(0,5,13,14) + \Sigma d(3,7,11)$  with a 4 to 1 Multiplexer and a minimum number of gates.



- b- Show how to make an 8 to 1 Mux by using a number of 4-to-1 Muxs and one 2-to-1 Mux.







**Question [5]: [ 12 mark]**

a) Derive the next state (characteristic) equation for T- Flip-Flop.

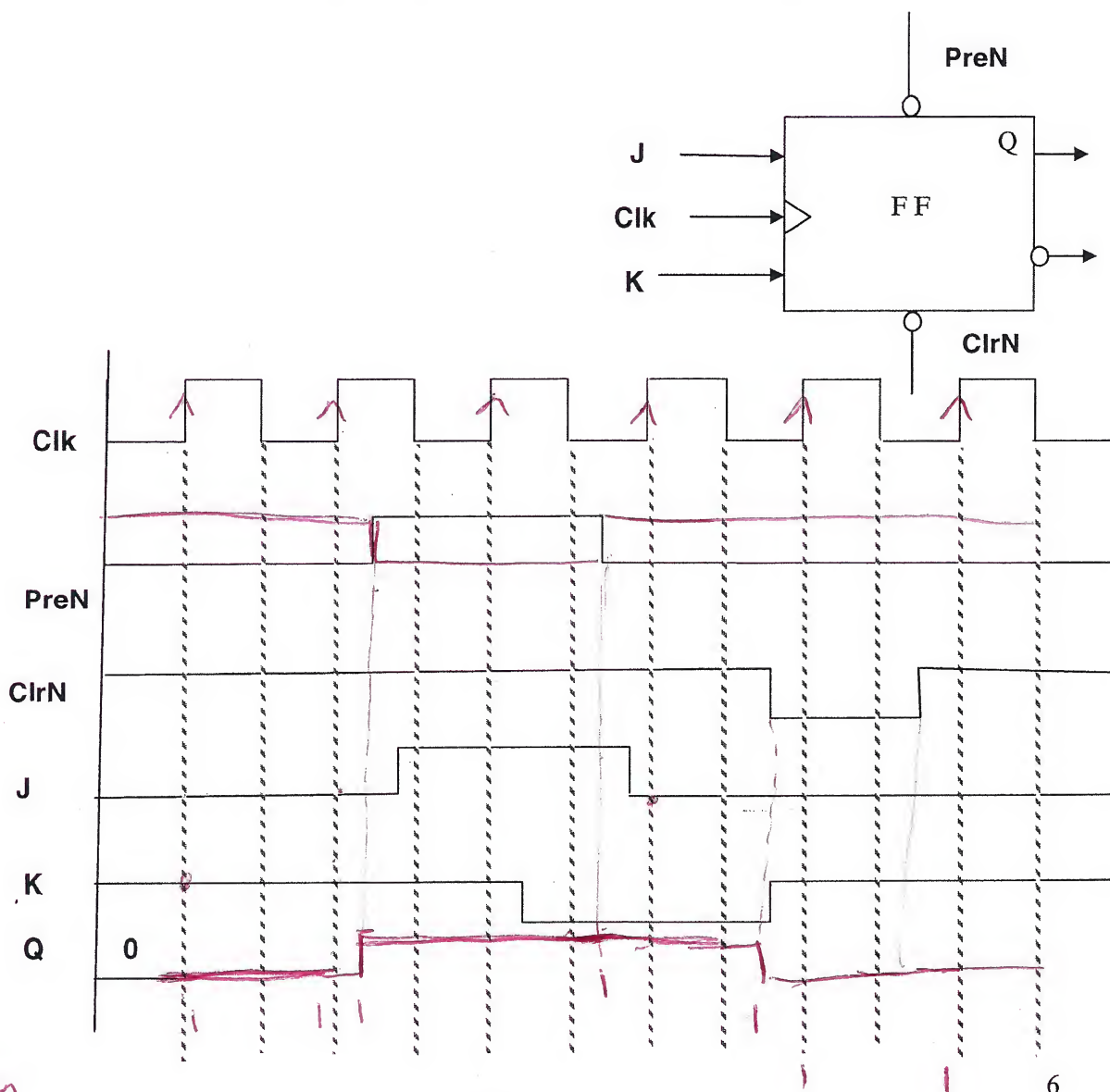
T	Q	Q <sup>+</sup>
0	0	0
0	1	1
1	0	1
1	1	0

$$Q^+ = T \oplus Q$$

(4)

(4)

b) Complete the following timing diagram for the following J-K Flip Flop.



J	K	Q
0	0	no change
0	1	0
1	0	1
1	1	Q

(8)